The Microprocessor-Based Synthesizer Controller

M. R. Wick

Radio Frequency and Microwave Subsystems Section

Implementation and performance of the new microprocessor-based controller and Dana Digiphase Synthesizer (DCO)* is presented. Since the previous report, six Synthesizer Controllers have been installed in the DSN exciter in the 64-meter and 34-meter subnets to support uplink tuning required for the Voyager-Saturn Encounter.

I. Introduction

The previous report describes the prototype Synthesizer Controller design features in control and monitor of a Dana Model 7010-S-241 Frequency Synthesizer. Subsequently, six production controllers have been installed in the 64-meter and 34-meter subnet (six stations) exciter to support the Voyager Project Saturn Encounter beginning in November 1980.

II. Implementation

The initial installation is a backup to the existing POCA and is under control of the Metric Data Assembly (MDA), as shown in Fig, 1. The need for an uplink tuning capability was given a greater emphasis because of the limited frequency tracking range of the Voyager 2 spacecraft receiver. The MDA was upgraded to incorporate a tuning capability including control of the existing Programmed Oscillator Control Assembly (POCA). The existing number of POCAs in the network, however, was insufficient to meet the needs, and additional controllers had to be built. The new Synthesizer

Controller was developed to supplement the POCA and provide improved performance such as that needed for uplink tuning: namely, additional ramp storage (100 ramps) and precision phase control during ramping (needed in doppler data processing).

In the presently implemented configuration with the MDA, frequency profile parameters (f,t) pairs, are received via the MDA and converted to the format required for the POCA (or new Synthesizer Controller). The POCA requires rate and time pairs (f_i, t_i) to produce a sequence of linear ramps and the Synthesizer Controller is designed to accept up to 100 ramps defined by frequency time pairs in the form $(\Delta f_i, \Delta t_i)$. Frequency and time increments are input to the Synthesizer Controller along with a beginning, or start frequency f_0. The Controller calculates the rate(s) f_i to an accuracy of 10^{-22} Hz/s to minimize the errors related to rate truncation. The additional rate resolution $(10^{-22}$ Hz/s) exceeds that of the existing POCA resolution capability $(10^{-5}$ Hz/s). The additional resolution was implemented in the design to minimize the ramp end-point frequency error due to truncation. This extended resolution was initially troublesome under control from the MDA because of the difference between the POCA and Synthesizer Controller. The MDA data interface for reporting the actual tuning rates provides for a maximum

---

*The combined capability of the Synthesizer Controller and Synthesizer is often referred to as a Digital Controlled Oscillator (DCO).

resolution of 10^{-5} Hz/s. The additional precision of the Synthesizer Controller was not being read out because of previously defined data format constraints. This additional precision resulted in a pseudo residual ramp error in the doppler data reduction process, and it was determined necessary to artificially limit the new Controller rate resolution.

This system deficiency will be corrected in a proposed firmware design change planned for implementing after Voyager 1 Saturn encounter. It will provide an additional (optional) capability to limit the resolution to 10^{-5} Hz/s. The proposed design change will permit an optional selection of the ramp resolution 10^{-5} Hz/s and retain the full resolution (10^{-22} Hz/s) for future use. In this revision to the firmware, the ramp rate is first calculated from the Δf_i, At, frequency increment and time increment pairs to a precision of 10^{-22} Hz/s and then rounded to 10^{-5} Hz/s. The target frequency change ($\Delta f_i'$) is then calculated to agree as determined from

$$\Delta \dot{f}_i' = f_i' (\Delta t_i)$$

The process is required to preserve the phase control accuracy of the ramp control algorithm. The difference between the commanded Δf_i and actual $\Delta f_i'$ is sufficiently small to be ignored for an eight hour tracking period. Figure 2 illustrates the effect of this roundoff procedure for a typical ramp.

III. Performance

Test data in tests conducted during the production of the six Controllers verified the design objective for phase control accuracy of 10^{-12} cycles in eight hours during ramping. Tests conducted require a phase error between a theoretical calculated value and the actual phase of no greater than ± 1 cycle. Tests included (1) a ramp over a period of eight hours using a ramp rate which covers the synthesizer tuning range (40-51 MHz) and (2) a ramp sequence using the maximum rate (± 100 kHz/s) over the tuning range.

References

1. Donnelly, H., Wick, M. R., et al., "The Microprocessor-Based Synthesizer Controller," in the *DSN Progress Report* 42-54, Jet Propulsion Laboratory, Pasadena, Calif., Dec. 15, 1979.

2. "Dana Model 7010-S-179 Digiphase Frequency Synthesizer," Dana Publication 980428-S-179, July 1971.
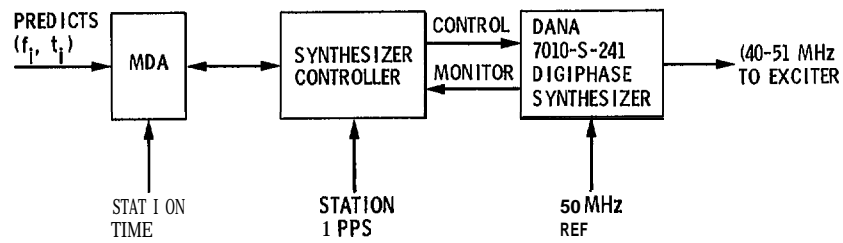
Fig. 1. Functional diagram, uplink tuning

NOTE:

$\dot{f}_1'$ DERIVED FROM $\dot{f}_1$
ROUNDED TO 10^{-5}
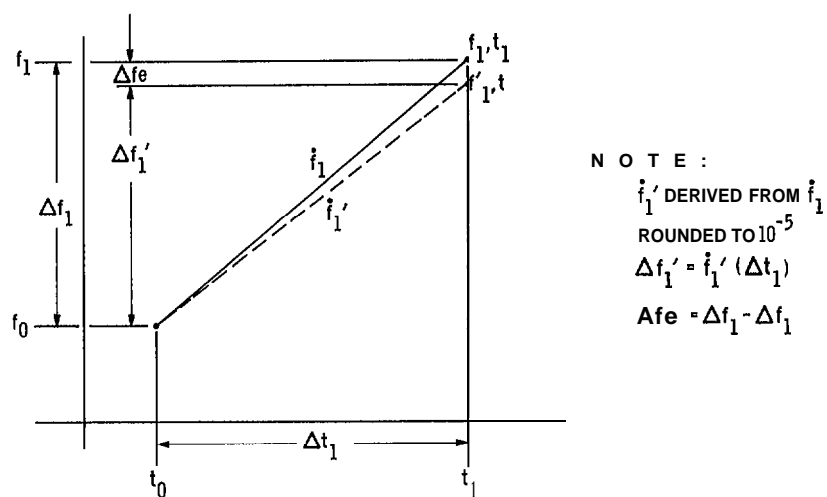
$\Delta f_1' = \dot{f}_1' \, (\Delta t_1)$

$Afe = \Delta f_1 - \Delta f_1$

Fig. 2. Ramp resolution (10^{-5} Hz/s vs 10^{-22} Hz/s)